WI61195

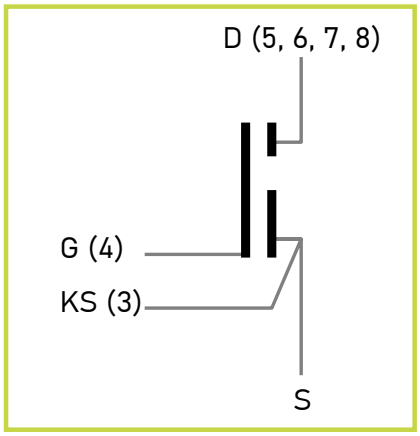
Discrete Power GaN IC

Description

The WI61195 is an enhancement mode GaN-on-silicon discrete power transistor of the WiseGan™ portfolio family of Wise-integration. The properties of GaN allow high current, high voltage breakdown and high switching frequency.

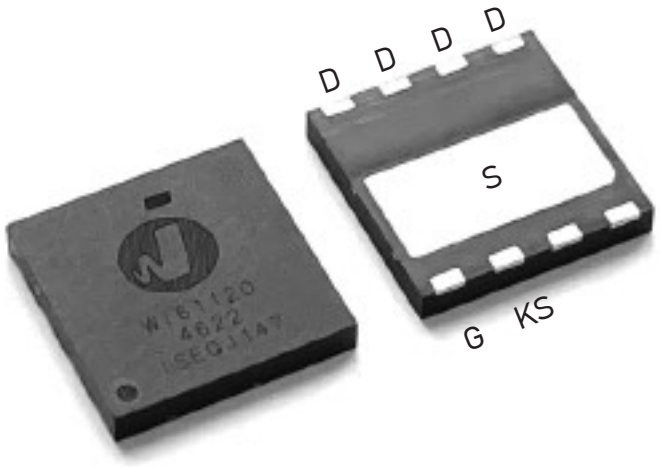
Applications

- High efficiency power conversion
- High density power conversion
- AC-DC, DC-DC, DC-AC
- Bridgeless Totem Pole PFC
- ACF (active clamp flyback)
- QRF (quasi resonant flyback)
- LLC resonant converter
- Half-bridge topologies
- Synchronous Buck or Boost
- Small-Medium UPS
- Fast Battery Charging



Features

- 650 V enhancement mode transistor
- Bottom-side cooled configuration
- $R_{DS(on)}$ = 195 mΩ
- $I_{DS(max)}$ = 8 A
- Low inductance PDFN package
- Easy gate drive requirements (0 V to 6 V)
- Transient tolerant gate drive up to 7 V
- High switching frequency (>1 MHz)
- Zero reverse recovery loss
- Small 8 x 8 mm PCB footprint



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Absolute Maximum Ratings

Parameter	Symbol	Value	Units
Drain-to-Source Transient Voltage [1]	V_{DS}	750	V
Gate-to-Source Transient Voltage [2]	V_{GS}	-2 to +7	V
Operating Junction Temperature	T_J	-40 to +150	°C
Operating Storage Temperature	T_{stg}	-55 to +150	°C

[1] maximum duration is 1ms
[2] maximum duration is 1µs

Operating conditions

Parameter	Symbol	Value	Units
Continuous Drain-to-Source Voltage	$V_{DS\ (max)}$	650	V
Gate-to-Source Voltage	V_{GS}	-1 to +6	V
Continuous Drain Current (T_J = 25°C)	I_D	8	A

Thermal Characteristics

Parameter	Symbol	Value	Units
Thermal Resistance (junction-to-case) – bottom side	$R_{\Theta JC}$	0.9	K/W
Thermal Resistance (junction-to-ambient)	$R_{\Theta JA}$	30.0	K/W

ESD Ratings

Parameter	Symbol	Value	Units
Human Body Model	HBM	1500	V
Charged Device Model	CDM	2000	V

Static Electrical Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS} = 6 V, T_J = 25 °C, I_{DS} = 2 A		195	225	mΩ
		V_{GS} = 6 V, T_J = 150 °C, I_{DS} = 2 A		380		mΩ
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, T_J = 25 °C, I_{DS} = 10 mA	0.9	1.3	1.75	V
		V_{DS} = V_{GS}, T_J = 150 °C, I_{DS}= 10 mA		1.8		V
Internal Gate Resistance	R_G	open drain		0.6		Ω
Drain-to-Source Leakage Current	I_{DSS}	V_{DS} = 650 V, V_{GS} = 0 V, T_J = 25°C		0.2	0.42	µA
		V_{DS} = 650 V, V_{GS} = 0 V, T_J = 150°C		6		µA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS} = 6 V, V_{DS} = 0 V, T_J = 25°C		22	50	µA
		V_{GS} = 6 V, V_{DS} = 0 V, T_J = 150 °C		200		µA
Source-to-Drain Reverse Voltage	V_{SD}	V_{GS} = 0 V, I_{SD} = 5 A		3.25		V
		V_{GS} = 0 V, I_{SD} = 6 A		3.55		V

Dynamic Electrical Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Units
Input Capacitance	C_{ISS}	V_{DS} =400 V, V_{GS} = 0V, f = 100 kHz		96.8		pF
Reverse Transfer Capacitance	C_{RSS}	V_{DS} =400 V, V_{GS} = 0V, f = 100 kHz		0.55		pF
Output Capacitance	C_{OSS}	V_{DS} =400 V, V_{GS} = 0V, f = 100 kHz		21.9		pF
Total Gate Charge	Q_G	V_{DS} = 400 V, V_{GS} = 0 V to 6 V		2.75		nC
Gate to Source Charge	Q_{GS}	V_{DS} = 400 V, V_{GS} = 0 V to 6 V		0.2		nC
Gate to Drain Charge	Q_{GD}	V_{DS} = 400 V, V_{GS} = 0 V to 6 V		1.2		nC
Output Charge	Q_{OSS}	V_{DS} = 400 V, V_{GS} = 0 V		24.2		nC
Output Capacitance Stored Energy	E_{OSS}	V_{DS} = 400 V, V_{GS} = 0 V		3.1		µJ
Effective Output Capacitance (Energy related)	$C_{O(ER)}$	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		38.9		pF
Effective Output Capacitance (Time related)	$C_{O(TR)}$	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		60.6		pF

Static main characteristics (T_J = 25°C unless otherwise noted)

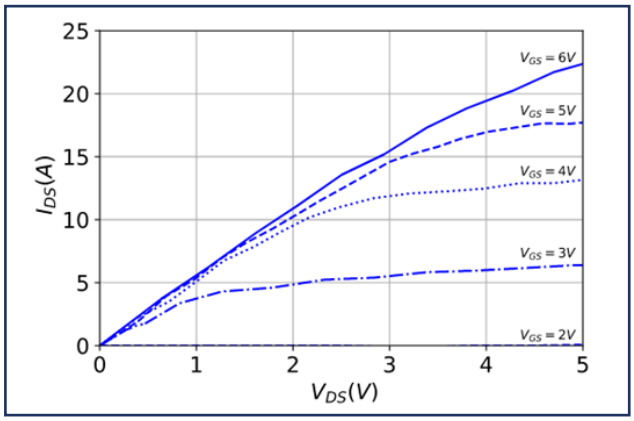


Figure 1. Output I_{DS} . V_{DS}

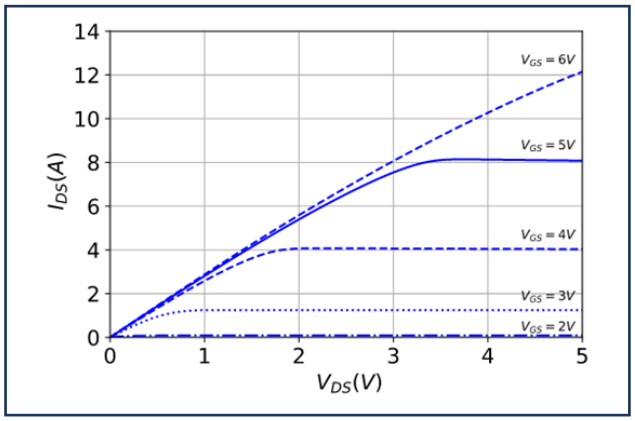


Figure 2. Simulated output I_{DS} . V_{DS} T_J = 125°C

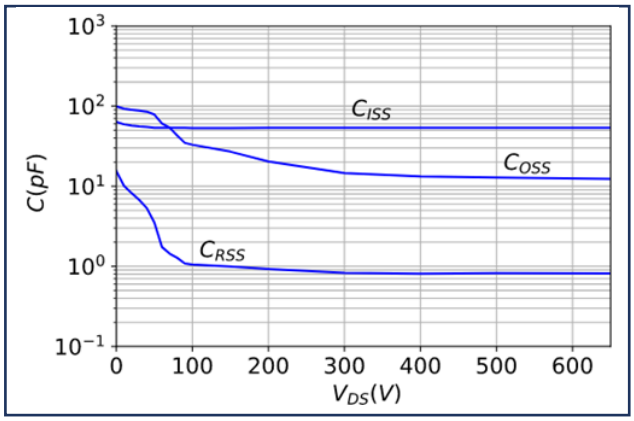


Figure 3. Capacitance

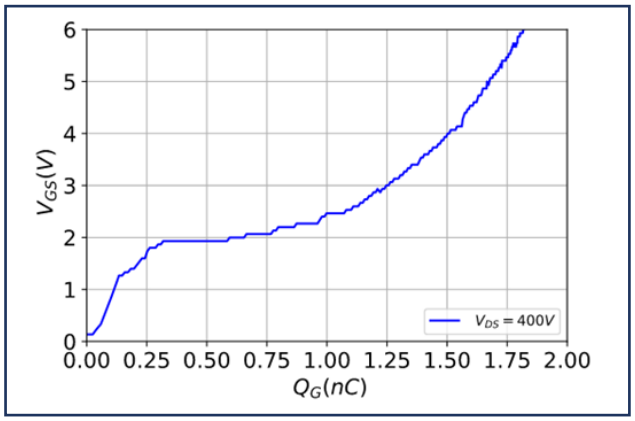


Figure 4. Gate Charge, Q_G

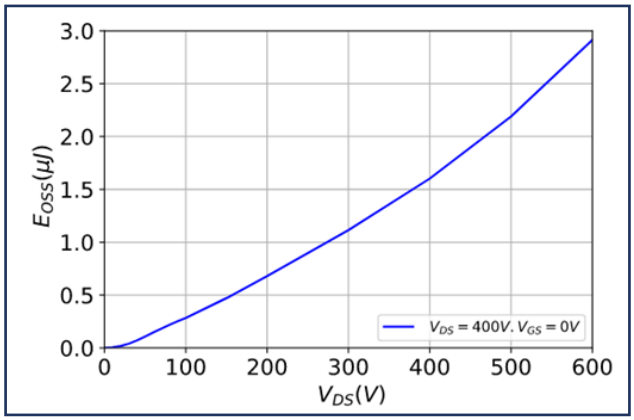


Figure 5. Stored Energy

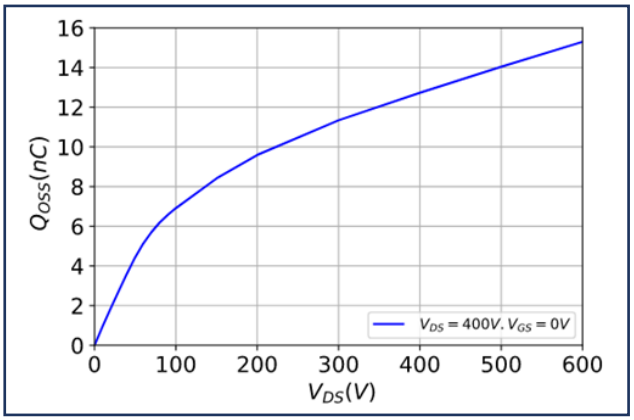


Figure 6. Output charge

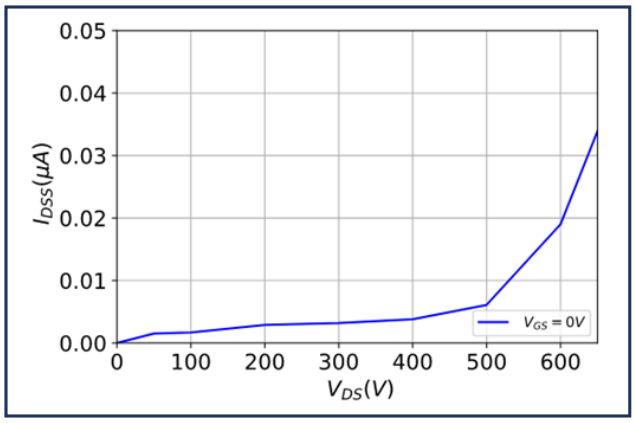


Figure 7. Drain-source leakage T_J = 25°C

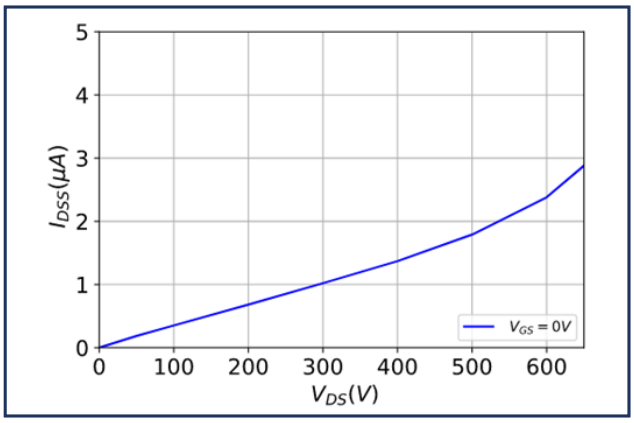


Figure 8. Drain-source leakage T_J = 125°C

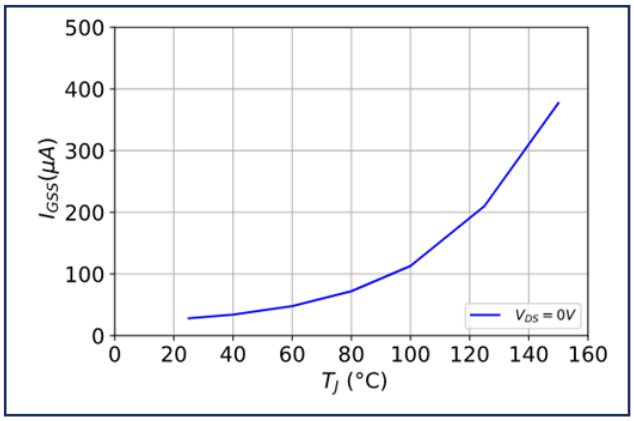


Figure 9. Gate-source leakage vs Temperature

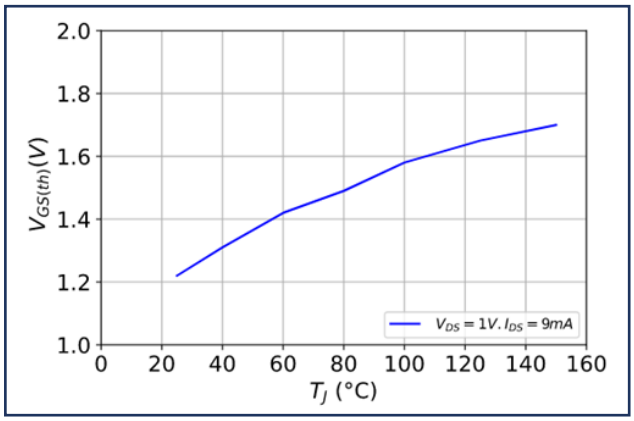


Figure 10. $V_{GS(th)}$ vs. Temperature

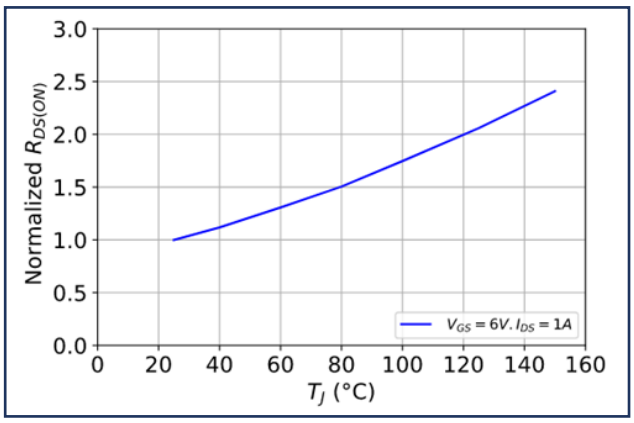


Figure 11. $R_{DS(ON)}$ vs. Temperature

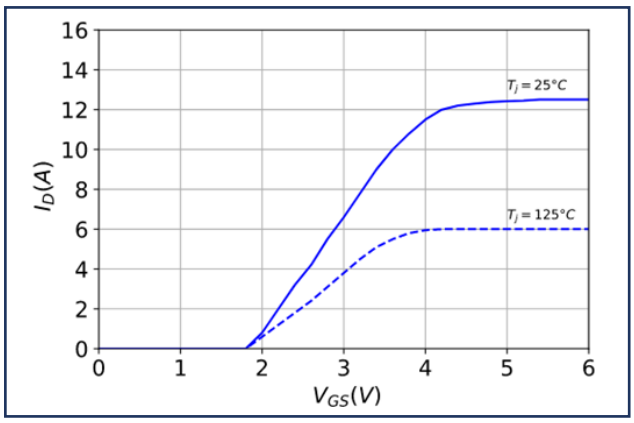


Figure 12. Transfer characteristics

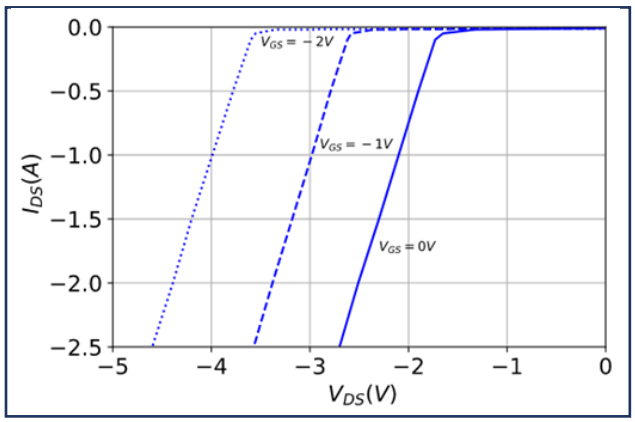


Figure 13. Reverse Conduction
T_J = 25°C

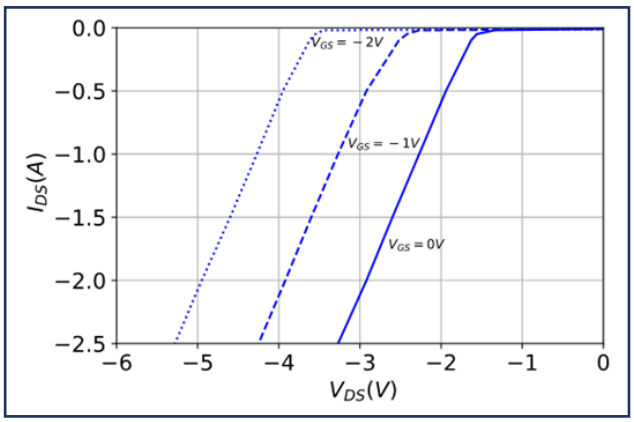
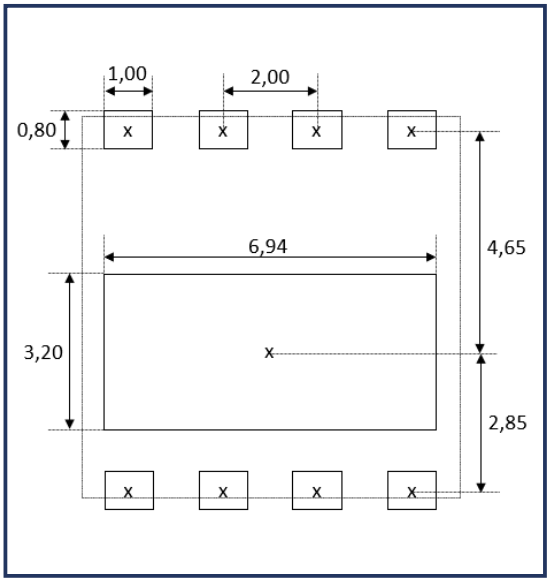


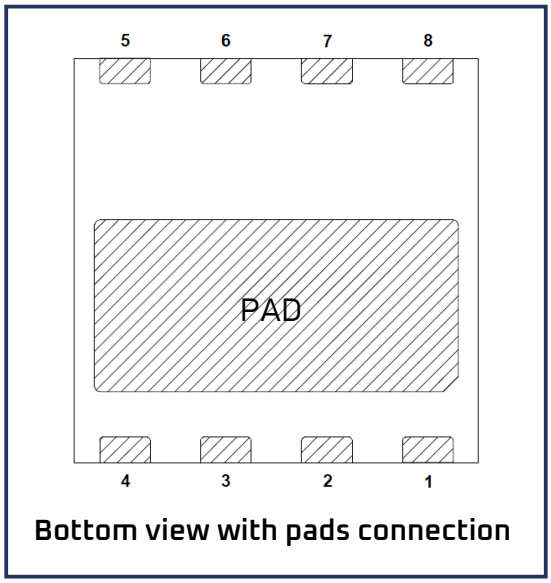
Figure 14. Reverse Conduction
T_J = 125°C

Package and Packing information

Land Pattern



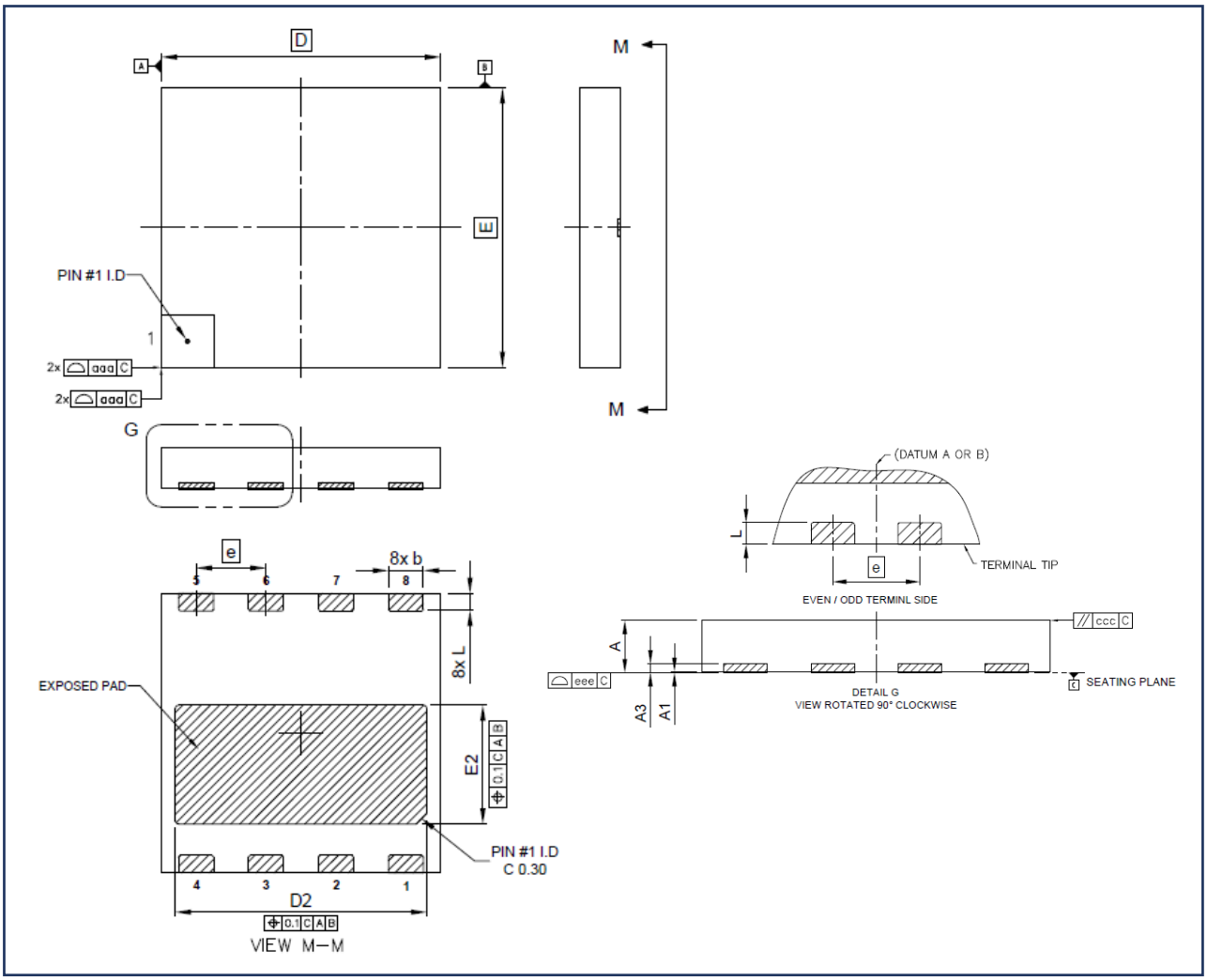
Pinout



Bottom view with pads connection

Number	Name	Function	Description
1		NC	Not connected internally, may be connected to the Source
2		NC	Not connected internally, may be connected to the Source
3	KS	Signal	Kelvin source of the GaN transistor
4	G	Signal	Gate of low side GaN transistor
5	D	Power	Drain of high side GaN transistor
6	D	Power	Drain of high side GaN transistor
7	D	Power	Drain of high side GaN transistor
8	D	Power	Drain of high side GaN transistor
PAD	S	Power	Source of the GaN transistor

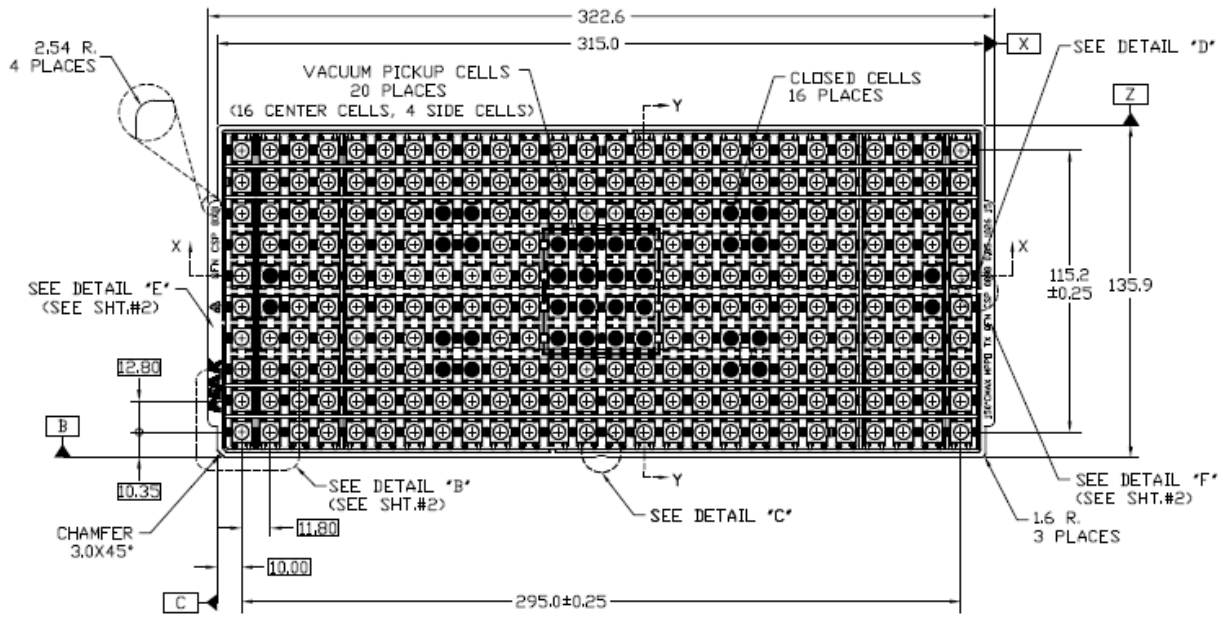
Package Outline Drawing



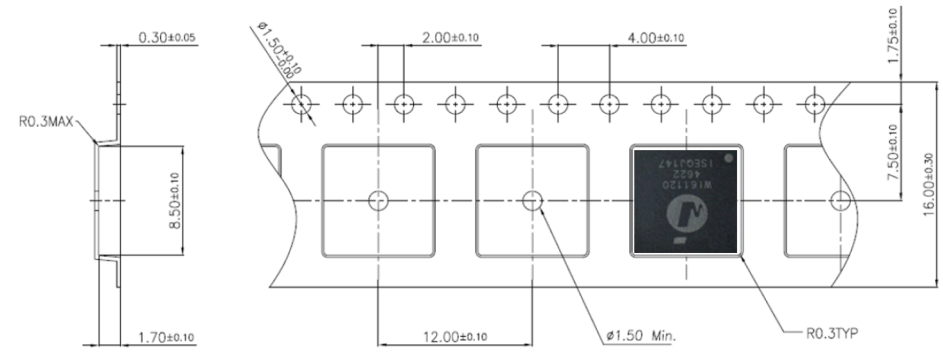
Dim	Min	Nom	Max	Unit
A	1.15	1.20	1.25	mm
A1	0.00		0.05	mm
A3		0.203 REF		mm
b	0.95	1.00	1.05	mm
D		8.00BSC		mm
E		8.00 BSC		mm
D2	7.10	7.20	7.30	mm
E2	3.30	3.40	3.50	mm

Dim	Min	Nom	Max	Unit
e		2.00 BSC		mm
L	0.45	0.50	0.55	mm
aaa		0.10		mm
bbb		0.10		mm
ccc		0.10		mm
ddd		0.05		mm
eee		0.08		mm

Tray dimensions (in mm)



Tape and Reel Dimensions (in mm)



NOTES:
1. 10 sprocket hole pitch cumulative tolerance ±0.2
2. Camber not to exceed 1mm in 100mm
3. Material: Black conductive Polystyrene
4. Ao and Bo measured on a plane 0.3mm above the bottom of the pocket
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.
7. Pocket center and pocket hole center must be same position.

Ordering Information

Ordering code	Package type	Packing method	Qty	Tray Qty	Box tray
WI61195T	8 x 8 mm PDFN	Tray	1300	26x10 parts	5
WI61195TR	8 x 8 mm PDFN	Tape and reel	2500	N/A	N/A