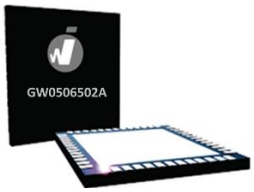
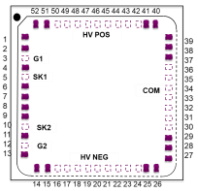
Features

- 650 V enhancement mode half bridge power switch
- Bottom-side cooled configuration
- $R_{DS(on)}$ = 100 mΩ per switch
- $I_{DS(max)}$ = 5 A
- Low inductance QFN PACKAGE
- Easy gate drive requirements (0 V to 6 V)
- Transient tolerant gate drive (-20 V / +10V)
- Very high switching frequency (> 10 MHz)
- Fast and controllable fall and rise times
- Integrated Source sense
- Reverse current capability
- Zero reverse recovery loss
- Small 8 x 8 mm^2 PCB footprint
- RoHS 6 compliant

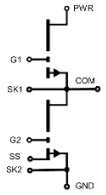


Package Outline



(Front View)

Circuit Symbol



Applications

- High efficiency power conversion
- High density power conversion
- AC-DC Converters
- Bridgeless Totem Pole PFC
- ZVS Phase Shifted Full Bridge
- Half Bridge topologies
- Synchronous Buck or Boost
- Small-Medium UPS
- Fast Battery Charging
- Class D Audio amplifiers

Description

The GW1006502A is an enhancement mode GaN-on silicon half bridge power circuit. The properties of GaN allow for high current, high voltage breakdown and high switching frequency.

Absolute Maximum Ratings per transistor (T_{case} = 25 °C except as noted)

Parameter	Symbol	Value	Unit
Operating Junction Temperature	T_J	-55 to +150	°C
Storage Temperature Range	T_S	-55 to +150	°C
Drain-to-Source Voltage	V_{DS}	650	V
Drain-to-Source Voltage - transient (note 1)	$V_{DS(transient)}$	750	V
Gate-to-Source Voltage	V_{GS}	-10 to +7	V
Gate-to-Source Voltage - transient (note 1)	$V_{GS(transient)}$	-20 to +10	V
Continuous Drain Current (T_{case} = 25 °C) (note 2)	I_{DS}	5	A
Continuous Drain Current (T_{case} = 100 °C) (note 2)	I_{DS}	4	A
Pulse Drain Current (Pulse width 100 µs)	$I_{DS\ Pulse}$	20	A

(1) Pulse ≤ 1 µs

(2) Limited by saturation

Thermal Characteristics (Typical values unless otherwise noted)

Parameter	Symbol	Value	Units
Thermal Resistance (junction-to-case) – bottom side	$R_{\Theta JC}$	2	°C /W
Thermal Resistance (junction-to-top)	$R_{\Theta JT}$	19	°C /W
Thermal Resistance (junction-to-ambient) (note 3)	$R_{\Theta JA}$	21	°C /W

Ordering Information

Ordering code	Package type	Packing method	Qty	Reel Diameter	Reel Width
GS1006502A	QFN 52 (8x8)	Tape-and-Reel	3000	13” (330mm)	16mm

Electrical Characteristics (Typical values at T_J = 25 °C, V_{GS} = 6 V unless otherwise noted per transistor)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Drain-to-Source Blocking Voltage	BV_{DS}	650			V	V_{GS} = 0 V I_{DSS} = 1 µA
Drain-to-Source On Resistance	$R_{DS(on)}$		100	110	mΩ	V_{GS} = 6 V, T_J = 25°C I_{DS} = 2 A
Drain-to-Source On Resistance	$R_{DS(on)}$		150		mΩ	V_{GS} = 6 V ,T_J = 150 °C I_{DS} = 2 A
Gate-to-Source Threshold	$V_{GS(th)}$	1.2	1.3	1.5	V	V_{DS} = V_{GS} , Tj=25°C I_{DS} = 1 mA
Gate-to-Source Current	I_{GS}		30		µA	V_{GS} = 6 V, V_{DS} = 0 V
Gate Plateau Voltage	V_{plat}		3		V	V_{DS} = 400 V I_{DS} = 5 A
Reverse Drain-to-Source voltage	V_{rDS}		1.3		V	V_{GS}=0V,Tj=25°C I_{SD} = 1 mA
Drain-to-Source Leakage Current	I_{DSS}		0.5	5	µA	V_{DS} = 650 V V_{GS} = 0 V T_J = 25 °C
Drain-to-Source Leakage Current	I_{DSS}		35	100	µA	V_{DS} = 650 V V_{GS} = 0 V T_J = 150 °C
Input Capacitance	C_{ISS}		120		pF	V_{DS} = 400 V V_{GS} = 0 V f = 100 kHz
Output Capacitance	C_{OSS}		25		pF	
Reverse Transfer Capacitance	C_{RSS}		1		pF	

(3) $C_{O(ER)}$ is the fixed capacitance that would give the same stored energy as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}

(4) $C_{O(TR)}$ is the fixed capacitance that would give the same charging time as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}.

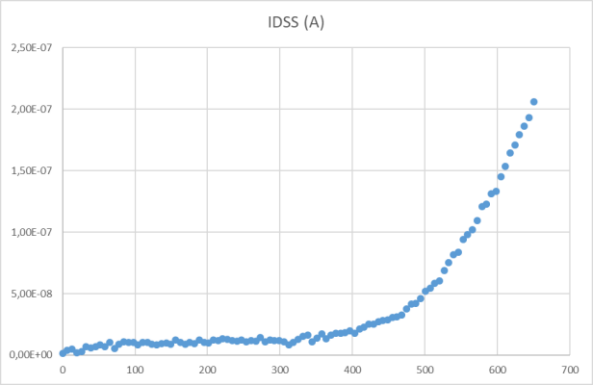


Figure 1 : Tenue en tension IDSS=f(BVDS,VGS=0V). à 650V, IDSS=0,2uA @ 25°C

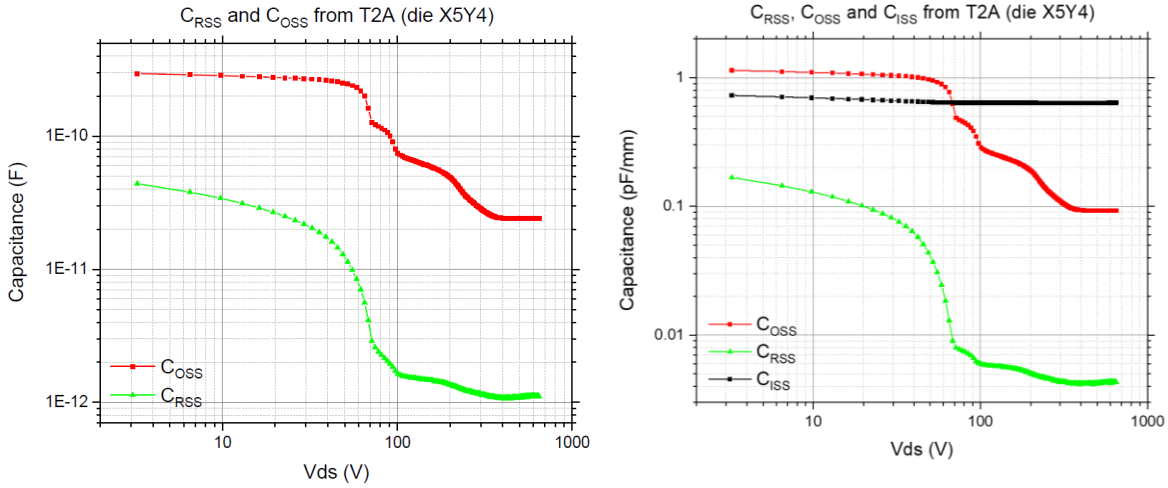


Figure 2 : Coss,Ciss et Crss en pF et en pf/mm.

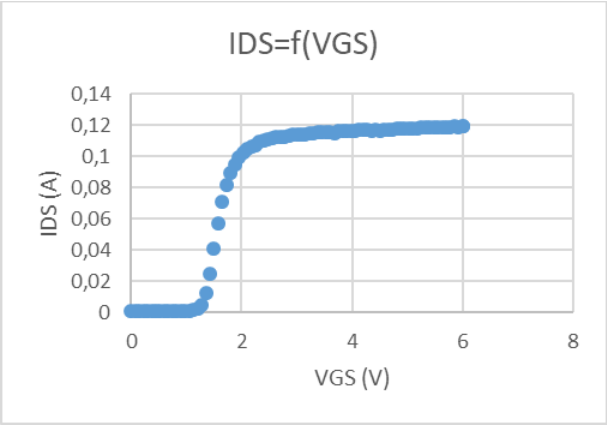


Figure 3 : Tension de seuil IDS=f(VGS) pour VDS=0,1V

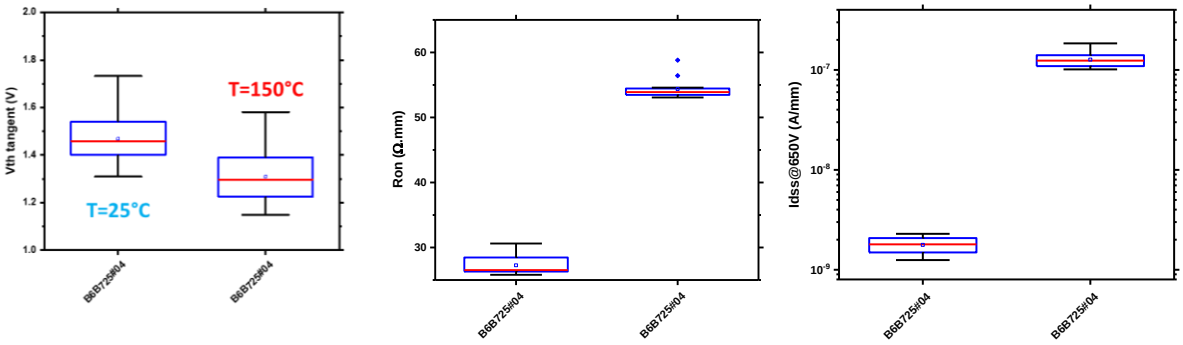


Figure 4 : Principales Caractéristiques en température 25°C et 150°C